Customer No.: 31561
Application No.: 10/711,473
Docket No.: 13530-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 1-18 and under 35 U.S.C. 103(a) as being unpatentable over Shih (US 2003/0230748) in view of Cho (KR 2002089981) and further in view of Peng (US 2004/0219723).

Claims 1 and 12 are amended and claim 19 is newly added. After entry of the foregoing amendments, claims 1-19 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicants respectfully traverse the rejection of claims 1-18 under 103(a) as being unpatentable over Shih (US 2003/0230748) in view of Cho (KR 2002089981) further in view of Peng (US 2004/0219723) because a prima facie case of obviousness has not been established by the Office Action.

> To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

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The present invention is in general related a low temperature polysilicon thin film transistor as claim 1 recites:

Claim 1. The low temperature polysilicon thin film transistor, comprising:
a substrate;
a polysilicon layer, disposed over the substrate, and the polysilicon layer comprising a source region, a drain region, a channel region between the source and drain regions and a lightly doped drain region between the channel region and the source and drain regions;
a gate insulation layer, disposed over the substrate covering the polysilicon layer;
a gate buffer layer, arranged over the gate insulation layer covering the channel region and the lightly doped drain region;
a gate, disposed over the gate buffer layer covering the channel region, wherein the gate buffer layer is disposed between the gate and the gate insulation layer;
a dielectric layer, arranged over the gate insulation layer covering the gate;
a drain metal layer, disposed over the dielectric layer and through the dielectric layer and the gate insulation layer to electrically connect with the drain region; and
a source metal layer, disposed over the dielectric layer and through the dielectric layer and the gate insulation layer to electrically connect with the source region.

The office action agrees that Cho fails to disclose the lightly doped drain regions. However, Shih discloses the lightly doped drain regions 309 in Figs. 3A-3G. Nevertheless, applicant respectfully submits even through Shih teaches the lightly doped drain regions and Cho discloses the buffer layer, Cho and Shih fail to teach ***the gate buffer layer*** is arranged over the gate insulation layer covering the channel region ***and the lightly doped drain*** as claim 1 recited. There is not any suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention.

In addition, in the Cho's reference, the gate electrode 101b is formed on the substrate 100, the buffer layer 102a is formed on the gate electrode 101b, and the dielectric layer 103 is formed

on the buffer layer 102a. In other words, the gate electrode 101b and the gate buffer layer 102a are sandwiched between the substrate 100 and the dielectric layer 103. However, in claim 1 of the present application, the gate insulating layer is disposed over the substrate, the gate buffer layer is disposed over the gate insulating layer, and the gate is formed over the gate buffer layer. The gate buffer layer and the gate insulating layer are sandwiched between the substrate and the gate. The relationship of the gate, the gate butter layer, the gate insulating layer and the substrate of claim 1 is different form the disclosure in the Cho reference.

Similarly, Peng also fails to teach the gate buffer layer as above mentioned, and therefore the three references combined do not teach each and every element in claim 1.

On the other hand, the present application also provides a method of fabricating a lightly doped drain region as claim 12 recites:

> Claim 12. The method of fabricating a lightly doped drain region, comprising:
> forming a polysilicon layer over a substrate;
> forming a gate insulation layer over the polysilicon layer;
> sequentially forming a gate buffer layer over the gate insulation layer and a gate over the gate buffer layer so that the gate buffer layer is formed between the gate and the gate insulation layer, wherein ***an edge portion of the gate buffer layer is exposed by the gate***; and
> ***performing a doping process to form a lightly doped drain region in the polysilicon layer underneath the exposed portion of the gate buffer layer.***

In the Shih's reference, the lightly doped drain regions 309 are formed by a trace N-type dopant implantation procedure ***with the gate conductive structure 308 as a mask*** (see paragraph [0034]). However, in claim 12 of the present application, ***the lightly doped drain region is***

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formed in the polysilicon layer underneath the exposed portion of the gate buffer layer. In other words, the lightly doped drain region of claim 12 is formed by a doping process **with the gate buffer layer as a mask**. Shih does not teach or suggest anything about the gate buffer layer, and thus Shih fails to teach the lightly doped drain region is formed in the polysilicon layer underneath the exposed portion of the gate buffer layer.

In addition, Cho also fails to teach or suggest that the lightly doped drain region is formed in the polysilicon layer underneath the exposed portion of the gate buffer layer. The device disclosed by Cho does not comprise lightly doped drain regions, and thus the step of forming the lightly doped drain regions is not disclosed in the Cho reference. Therefore, both Shih and Cho fail to teach or suggest the step of performing a doping process to form ***a lightly doped drain region*** in the polysilicon layer ***underneath the exposed portion of the gate buffer layer*** as claim 12 recited.

Similarly, Peng also fails to teach the step of performing a doping process to form a lightly doped drain region in the polysilicon layer underneath the exposed portion of the gate buffer layer as above mentioned, and thus the three references combined do not teach each and every element in claim 12.

Furthermore, Shih teaches a TFT structure but there is not a gate buffer layer in the structure. Cho discloses forming a buffer layer 101b on the gate 102b in a gate pad area, and the gate pad area is not a TFT structure. A patent claim is obvious, and thus invalid, when the differences between the claimed invention and the prior art "***are such that the subject matter as***

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a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103; see also Graham v. John Deere Co., 383 U.S. 1, 14, 86 S. Ct. 684, 15 L. Ed. 2d 545 (1966); In re Dembiczak, 175 F.3d 994, 998 (Fed. Cir. 1999).

For at least the foregoing reasons, Applicant respectfully submits a prima facie case of obviousness has not been established by the Office Action. Independent claims 1 and 12 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-11, 13-18 patently define over the prior art as well.

Newly added claim 19

Applicant has further newly added claim 19 with the limitation of "the gate buffer layer is arranged over the channel region and the lightly doped drain ***and is not disposed over the source and the drain***". Applicant respectfully submits the three references cited do not teach the feature.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-19 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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